IN THE CLAIMS:

1.-2. (canceled)

3. (currently amended) The method of ~~reproducing~~reading a mark on a semiconductor wafer according to claim 2~~6~~, wherein the ~~at least partially-effaced~~second mark is reproduced by means of forming ~~a~~said second mark ~~similar~~identical to the ~~partially-effaced~~ mark at ~~another~~a second location spaced apart from the ~~partially-effaced~~first mark.

4. (currently amended) The method of ~~reproducing~~reading a mark on a semiconductor wafer according to claim 2~~6~~, wherein the ~~partially-effaced~~first mark is reproduced by means of forming a second mark ~~similar~~identical to the ~~partially-effaced~~first mark at ~~another~~a second location in the vicinity of the ~~partially-effaced~~first mark.

5. (currently amended) The method of ~~reproducing~~reading a mark on a semiconductor wafer according to claim 2~~6~~, wherein the ~~predetermined~~second mark is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and the ~~partially-effaced~~first mark is reproduced by means of forming a second mark ~~similar~~identical to the ~~partially-effaced~~first mark at ~~another~~a second location in the vicinity of the ~~partially-effaced~~first mark.

6. (currently amended) The method of ~~reproducing~~reading a mark on a semiconductor wafer according to claim 2~~6~~, wherein the ~~predetermined~~second mark is a minute ID mark which is assigned to the semiconductor wafer and is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and the ~~partially-effaced~~first mark is reproduced by means of forming a second mark ~~similar~~identical to the ~~partially-effaced~~first mark at ~~another~~a second location in the vicinity of the ~~partially-effaced~~first mark.

7.-12. (canceled)

13. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein two or more similar~~The method of claim 26 further including the step of providing said first and second marks ~~are provided~~ at positions where the marks are to undergo the same surface treatment at different speeds during the course of manufacture.

14. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more similar~~The method of claim 26 further including the step of providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similara~~ third marks ~~are provided~~ on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture.

15. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more similar~~The method of claim 26 further including the step of providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similara~~ third marks ~~are provided~~ on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks are located close to each other and such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture.

16. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more similar~~The method of claim 26 further including the step of providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similara~~ third marks ~~are provided~~ on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface

treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

17. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein two or more similar~~The method of claim 26 further including the step of forming the first and second marks ~~are formed~~ by means of a combination of dots, each dot measuring 1 to 13 μm wide, and ~~some of two or more similar~~providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similar~~a third marks ~~are~~ is provided on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

18. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein two or more similar~~The method of claim 26 further including the step of assigning said first and second marks ~~are minute~~as ID marks ~~which are assigned~~ to the semiconductor wafer ~~and are formed by means of~~as a combination of dots, each dot measuring 1 to 13 μm wide, ~~and some of two or more similar~~providing said first marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similar~~said third mark identical to said first and second marks ~~are provided~~ on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

19. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein two or more similar~~The method of claim 26 further including the step of assigning ID marks to said first and second marks ~~are minute ID marks which are assigned~~ to the semiconductor wafer, ~~are formed~~and forming said ID marks by ~~means of~~ a combination of dots, each dot measuring 1 to 13 μm, ~~and are~~ affixeding said ID marks on the interior wall surface of a notch, and ~~some of two or more similar~~providing said first marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similar~~a third marks ~~are provided~~identical to said first and second marks on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

20. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein two or more similar~~The method of claim 26 further including the steps of forming said first and second marks ~~are formed~~ by means of a combination of dots, each dot measuring 1 to 13 μm for positioning purpose, and ~~some of two or more similar~~providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similar~~a third marks ~~are provided~~identical to said first and second mark on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

21. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein two or more similar~~The method of claim 26 further including the steps of forming first and second marks ~~are formed~~ by means of a combination of dots, each dot measuring 1 to 13 μm and indicateing a crystal orientation of the semiconductor wafer, and ~~some of two or more similar~~providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similar~~a third marks ~~are provided~~identical to said first and second marks on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

22. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12~~The method of claim 26, wherein the semiconductor wafer is perfectly annular; ~~two or more similar~~and including the steps of forming first and second identical marks ~~are formed~~ by means of a combination of dots, each dot measuring 1 to 13 μm and indicateing crystal orientation of the semiconductor wafer; and ~~some of two or more similar~~providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similar~~providing a third marks ~~are provided~~identical to said first and second marks on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

23. (currently amended) ~~The semiconductor wafer for distribution purpose according to claim 12, wherein two or more similar~~The method of claim 26 further including the steps of aligning said first and second marks ~~are aligned~~ in a single direction; and ~~some of two or more similar~~providing said first and second marks ~~are provided~~ on the front side of the semiconductor wafer and ~~the other similar~~providing a third marks ~~are provided~~identical to said first and second marks on the reverse side of ~~the same~~said semiconductor wafer, such that the first, second and third marks undergo the same surface treatment at different speeds during the course of manufacture and such that the first, second and third marks are located within an area where a single optical reading machine can read the first, second and third marks simultaneously.

24.-25. (canceled)

26. (new) A method of reading a mark on a semiconductor wafer, comprising the steps of:

forming a first mark separate and distinct from a second mark, each of said first and second marks having an identical content and being in an identical format on an interior wall of a notch of each of a plurality of said semiconductor wafers;

storing the plurality of semiconductor wafers in a wafer carrier by aligning said notches; and

simultaneously reading the first and second marks on the interior wall of said notch by an optical reader.